	Search Text
1	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and @ad<"20040329" and "716"/$.ccls. and shape same (module block cell) and boundar$5 same (module block cell)
2	(pld fpga field near3 array programmable near4 logic near4 device) and floor$7 and @ad<"20040329" and "716"/$.ccls. and shape same (module block cell) and boundar$5 same (module block cell) and (overlap$8 non adj overlap$8 nonoverlap$6)
3	(pld programmable near4 logic near4 decive) same (fpga field near4 array near4 programmable)
4	(pld programmable near4 logic near4 decive) same (fpga field near4 array near4 programmable) and @ad<"20040329"
5	(pld programmable near4 logic near4 decive) same (fpga field near4 array near4 programmable) same (known called) and @ad<"20040329"
6	(pld programmable near4 logic near4 decive) with (fpga field near4 array near4 programmable) with (known called) and @ad<"20040329"
7	(pld programmable near4 logic near4 decive) with (fpga field near4 array near4 programmable) with (known called) and @ad<"20040329" and "716"/$.ccls.
8	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4)
9	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls.
10	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 ovelap$6)
11	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6)
12	(pld fpga programmable near4 (field logic array device)) same (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 dimension)
13	(pld fpga programmable near4 (field logic array device)) same (floor$7 plac$6 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 dimension)
14	(pld fpga programmable near4 (field logic array device)) same (floor$7 plac$6 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 geometry dimension)

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15	"6490717".pn. and (pld fpga programmable near4 (field logic array device)) and (cell block module)
16	"6490717".pn. and (pld fpga programmable near4 (field logic array device)) and (cell block module)
17	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693").pn.
18	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693").pn.
19	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5818729" "5778216" "6002857").pn.
20	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5818729" "5778216" "6002857" "5483461" "6134702" "5309371").pn.
21	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn.
22	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn. and (pld fpga)
23	"20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn. and (pld fpga) and plac$5 same rout$5
24	("20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn.) and (pld fpga) and plac$5 same rout$5
25	("20020166098" ("5808330" "5930499" "5953236" "6766500" "6817005" "5822214" "5818729" "5778216" "6002857" "6301693" "5483461" "6134702" "5309371").pn.) and (pld fpga) and plac$5 same rout$5 and (ovelap$5 boundar$4) same (cell block module)
26	(pld fpga programmable near4 (field logic array device)) and (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6)
27	(pld fpga programmable near4 (field logic array device)) and (floor$7 partition$4 divi$6) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6) and (module block cell) with (siz$4 shap$4 dimension$4 geometry width height)
28	(pld fpga programmable near4 (field logic array device)) and (adjust$4 modif$6) same (module block cell) same (boundar$4 shape siz$4 dimension) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and (module block cell) same (boundar$4 border ovelap$6) and (module block cell) with (shape siz$4 dimension)
29	fixed same (module block cell) same (floo$6) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6) and (module block cell) with (siz$4 shap$4 dimension$4 geometry width height)

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30	fixed same (module block cell) same (floo$6) same (boundar$4 border$4 ovelap$6 nonoverlap$5) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6) and (module block cell) with (siz$4 shap$4 dimension$4 geometry width height)
31	fixed same (module block cell) same (boundar$4 border$4 ovelap$6 nonoverlap$5) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6) and (module block cell) with (siz$4 shap$4 dimension$4 geometry width height)
32	fixed same (module block cell) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (module pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block cell) same (boundar$4 border$4 ovelap$6) and (module block cell) with (siz$4 shap$4 dimension$4 geometry width height)
33	(module block) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (module pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls and (module block) with (siz$4 shap$4 dimension$4 geometry width height) and (plac$6 layout$6) same (solution feasib$6)
34	"716"/$.ccls and (module block) with (siz$4 shap$4 dimension$4 geometry width height) and (plac$6 layout$6) same (solution feasib$6) and @ad<"20040329"
35	(module block) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (module pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls. and (module block) with (siz$4 shap$4 dimension$4 geometry width height) and (plac$6 layout$6) same (solution feasib$6)
36	"20040194048" and (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4)
37	"20040194048" and (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4)
38	"20020073380" and (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4)
39	(module block) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (module pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls and hard$6 same (module constrain$4) and soft$6 same (module constrain$4)
40	(module block) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4) same (floor$6 plac$7 layout$4) and (pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls
41	rectangle same (plac$6 layout) and "716"/$.ccls. and @ad<"20040329"

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42	rectangle same (plac$6 layout) and "716"/$.ccls. and @ad<"20040329" and fixed same (block module)
43	rectangle same (plac$6 layout) and "716"/$.ccls. and @ad<"20040329" and fixed same (rectangle block module) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block rectangle)
44	(rectangle module) same (plac$6 layout) and "716"/$.ccls. and @ad<"20040329" and unchanged same (rectangle block module) and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block rectangle)
45	slic$4 same (flloor$5 (pld fpga programmable near4 (field logic array device))) and floor$4 same (slic$5 pld fpga programmable near4 (field logic array device))
46	slic$4 same (flloor$5 (pld fpga programmable near4 (field logic array device))) and floor$4 same (slic$5 pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls.
47	slic$4 same (flloor$5 (pld fpga programmable near4 (field logic array device))) and floor$4 same (slic$5 pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls. and (module block) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4)
48	simulat$5 with anneal$4 and (module rectangle block) with (siz$4 shap$4 dimension$4 geometry width height) and @ad<"20040329" and "716"/$.ccls.
49	simulat$5 with anneal$4 and (module rectangle block) with (siz$4 shap$4 dimension$4 geometry width height) and @ad<"20040329" and "716"/$.ccls. and (pld fpga programmable near4 (field logic array device)) and (floor$7)
50	((rectangle module block) same (plac$6 layout) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4)).ab. and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (module pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls.
51	((rectangle module block) same (floor$8) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4)).ab. and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (module pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls.
52	((rectangle module block) same (plac$6 layout) same (boundar$4 border$4 ovelap$6 nonoverlap$5 non adj overlap$4)).ab. and (pld fpga programmable near4 (field logic array device)) and (floor$7) same (module block cell) and (module pld fpga programmable near4 (field logic array device)) same (plac$6 same rout$4) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls. and (module block rectangle) with (siz$4 shap$4 dimension$4 geometry width height)
53	((rectangle module block) same (floor$6 plac$6 layout$5) same (free eliminat$4 avoid$4)) same overlap$6 and (pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls.
54	(pld fpga programmable near4 (field logic array device)) and (simulat$5 with anneal$4) same (cost$4 optim$6) and (module rectangle block) with (siz$4 shap$4 dimension$4 geometry width height) and @ad<"20040329" and "716"/$.ccls. and (pld fpga programmable near4 (field logic array device)) and (floor$7)

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55	(pld fpga programmable near4 (field logic array device)) and (simulat$5 with anneal$4) same (cost$4 optim$6) and (module rectangle block) with (siz$4 shap$4 dimension$4 geometry width height) and @ad<"20040329" and "716"/$.ccls. and (pld fpga programmable near4 (field logic array device)) and (floor$7) and (ovelap$6 nonoverlap$5 non adj overlap$4) same (module rectangle block)
56	cost and anneal$4 and optima$6 and (overlap$5 non adj overlap$6)
57	cost and anneal$4 and optima$6 and (overlap$5 non adj overlap$6) and (pld fpga programmable near4 (field logic array device)) and (module rectangle block) with (siz$4 shap$4 dimension$4 geometry width height) and @ad<"20040329" and "716"/$.ccls.
58	cost and anneal$4 and optima$6 and (overlap$5 non adj overlap$6) and (pld fpga programmable near4 (field logic array device)) and (module rectangle block) with (siz$4 shap$4 dimension$4 geometry width height) and @ad<"20040329" and "716"/$.ccls. and (netlist net adj list)
59	"5309371".pn. and (modif$5 alter$4 chang$6)
60	(rectangle module block) same (floor$6 plac$6 layout$5) same (nonoverlap$5 non adj overlap$6) overlap$6 and (pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls. and (module block rectangle) with (siz$4 shap$4 dimension$4 geometry width height) and floor$6 and netlist near4 (alter$4 chang$5 modif$6)
61	(rectangle module block) same (floor$6 plac$6 layout$5) same (nonoverlap$5 non adj overlap$6 overlap$6) and (pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls. and (module block rectangle) with (siz$4 shap$4 dimension$4 geometry width height) and floor$6 and netlist near4 (alter$4 chang$5 modif$6)
62	(rectangle module block) same (nonoverlap$5 non adj overlap$6 overlap$6) and (pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls. and (module block rectangle) with (siz$4 shap$4 dimension$4 geometry width height) and floor$6 and netlist near4 (alter$4 chang$5 modif$6)
63	(rectangle module block) same (nonoverlap$5 non adj overlap$6 overlap$6) and (pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls. and (module block rectangle) with (siz$4 shap$4 dimension$4 geometry width height) and floor$6 and netlist same (alter$4 chang$5 modif$6)
64	"20020073380" and floor$6
65	"20020073380" and (overlap$5 non adj overlap$6 boundar$6)
66	pld same fpga same (known conventional standard) and @ad<"20040329" and "716"/$.ccls.
67	pld with fpga with (known conventional standard) and @ad<"20040329" and "716"/$.ccls.
68	"5309371".pn. and (pld programmable)
69	kernel and percent$4 same (block module)
70	kernel and percent$4 same (block module) and @ad<"20040329" and "716"/$.ccls.
71	percent$4 same (block module) same (alter$4 chang$5 adjust$5) and @ad<"20040329" and "716"/$.ccls.
72	percent$4 same (block module) same (alter$4 modif$6 chang$5 adjust$5) and @ad<"20040329" and "716"/$.ccls.

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73	percent$4 same (block module) same (alter$4 modif$6 chang$5 adjust$5) same (art known conventional standard) and @ad<"20040329" and "716"/$.ccls.
74	"20040194048" and (overlap$5 non adj overlap$6 boundar$6)
75	(rectangle module block) same (nonoverlap$5 non adj overlap$6 overlap$6) and (pld fpga programmable near4 (field logic array device)) and @ad<"20040329" and "716"/$.ccls.and "716"/$.ccls. and (module block rectangle) with (siz$4 shap$4 dimension$4 geometry width height) and floor$6 and (chang$4 modif$5) near3 (part$4 portion)
76	"6086631".pn. and (siz$4 shap$4 dimension$4 geometry width height)